

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANTS:

Fitzgerald et al.

SERIAL NUMBER:

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ART UNIT:

2818

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EXAMINER:

Dung Anh Le

TITLE:

METHOD OF FABRICATING CMOS INVERTER AND INTEGRATED

CIRCUITS UTILIZING STRAINED SILICON SURFACE CHANNEL

MOSFETS

Mail Stop Amendment Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

RESPONSE

Sir:

In response to the Office action mailed on February 18, 2004, Applicants request the Examiner to consider the following:

Remarks begin on page 2 of this paper; and

Conclusion begins on page 2 of this paper.